

DDR2 Registered SDRAM MODULE

240pin Registered Module based on 1Gb A-die

72-bit ECC

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Table of Contents

| | |
|--|----|
| 1.0 DDR2 Registered DIMM Ordering Information | 4 |
| 2.0 Features | 4 |
| 3.0 Address Configuration | 4 |
| 4.0 Pin Configurations (Front side/Back side) | 5 |
| 5.0 Pin Description | 5 |
| 6.0 Input/Output Function Description | 6 |
| 7.0 Functional Block Diagram..... | 7 |
| 7.1 1GB, 128Mx72 Module (M393T2863AZ3/M393T2863AZA) | 7 |
| 7.2 2GB, 256Mx72 Module (M393T5663AZ3/M393T5663AZA) | 8 |
| 7.3 2GB, 256Mx72 Module (M393T5660AZ3/M393T5660AZA) | 9 |
| 7.4 4GB, 512Mx72 Module (M393T5168AZ0/M393T5166AZA) | 10 |
| 8.0 Absolute Maximum DC Ratings | 11 |
| 9.0 AC & DC Operating Conditions | 11 |
| 9.1 Operating Temperature Condition | 12 |
| 9.2 Input DC Logic Level | 12 |
| 9.3 Input AC Logic Level | 12 |
| 9.4 AC Input Test Conditions | 12 |
| 10.0 IDD Specification Parameters Definition | 13 |
| 11.0 Operating Current Table(1-1)..... | 14 |
| 11.1 M393T2863AZ3/M393T2863AZA : 1GB(128Mx8 *9) Module | 14 |
| 11.2 M393T5663AZ3/M393T5663AZA : 2GB(128Mx8 *18) Module | 14 |
| 11.3 M393T5660AZ3/M393T5660AZA : 2GB(256Mx4 *18) Module | 15 |
| 11.4 M393T5168AZ0/M393T5166AZA : 4GB(st.512Mx4 *18) Module | 15 |
| 12.0 Input/Output Capacitance | 16 |
| 13.0 Electrical Characteristics & AC Timing for DDR2-667/533/400..... | 17 |
| 13.1 Refresh Parameters by Device Density | 17 |
| 13.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin | 17 |
| 13.3 Timing Parameters by Speed Grade | 17 |
| 14.0 Physical Dimensions..... | 19 |
| 14.1 128Mbx8 based 128Mx72 Module(1 Rank) (M393T2863AZ3/M393T2863AZA) | 19 |
| 14.2 128Mbx8/256Mbx4 based 256Mx72 Module(2/1 Ranks) (M393T5663AZ3/M393T5663AZA/ M393T5660AZ3/M393T5660AZA) | 20 |
| 14.3 st.512Mbx4 based 512Mx72 Module(2 Ranks) (M393T5168AZ0/M393T5166AZA)..... | 21 |
| 15.0 240 Pin DDR2 Registered DIMM Clock Topology | 22 |

Revision History

| Revision | Month | Year | History |
|----------|-------|------|------------------------------------|
| 1.0 | July | 2005 | - Initial Release |
| 1.1 | Aug. | 2005 | - Revised IDD Current Values |
| 1.2 | Sep. | 2005 | - Revised the Ordering Information |
| 1.3 | Apr. | 2006 | - Revised IDD Current Values |

1.0 DDR2 Registered DIMM Ordering Information

| Part Number | Density | Organization | Component Composition | Number of Rank | Parity Register | Height |
|------------------------|---------|--------------|----------------------------|----------------|-----------------|--------|
| M393T2863AZ3-CD5/CC | 1GB | 128Mx72 | 128Mx8(K4T1G084QA)*9EA | 1 | X | 30mm |
| M393T2863AZA-CE6/D5/CC | 1GB | 128Mx72 | 128Mx8(K4T1G084QA)*9EA | 1 | O | 30mm |
| M393T5663AZ3-CD5/CC | 2GB | 256Mx72 | 128Mx8(K4T1G084QA)*18EA | 2 | X | 30mm |
| M393T5663AZA-CE6/D5/CC | 2GB | 256Mx72 | 128Mx8(K4T1G084QA)*18EA | 2 | O | 30mm |
| M393T5660AZ3-CD5/CC | 2GB | 256Mx72 | 256Mx4(K4T1G044QA)*18EA | 1 | X | 30mm |
| M393T5660AZA-CE6/D5/CC | 2GB | 256Mx72 | 256Mx4(K4T1G044QA)*18EA | 1 | O | 30mm |
| M393T5168AZ0-CD5/CC | 4GB | 512Mx72 | st.512Mx4(K4T2G064QA)*18EA | 2 | X | 30mm |
| M393T5166AZA-CE6/D5/CC | 4GB | 512Mx72 | st.512Mx4(K4T2G264QA)*18EA | 2 | O | 30mm |

Note: "Z" of Part number(11th digit) stand for Lead-free products.

Note: "3" of Part number(12th digit) stand for Dummy Pad PCB products.

Note: "A" of Part number(12th digit) stand for Parity Register products.

2.0 Features

- Performance range

| | E6(DDR2-667) | D5(DDR2-533) | CC(DDR2-400) | Unit |
|-------------|--------------|--------------|--------------|------|
| Speed@CL3 | 400 | 400 | 400 | Mbps |
| Speed@CL4 | 533 | 533 | 400 | Mbps |
| Speed@CL5 | 667 | 533 | - | Mbps |
| CL-tRCD-tRP | 5-5-5 | 4-4-4 | 3-3-3 | CK |

- JEDEC standard 1.8V ± 0.1V Power Supply
- $V_{DDQ} = 1.8V \pm 0.1V$
- 200 MHz f_{CK} for 400Mb/sec/pin, 267MHz f_{CK} for 533Mb/sec/pin, 333MHz f_{CK} for 667Mb/sec/pin
- 8 Banks
- Posted \overline{CAS}
- Programmable \overline{CAS} Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination with selectable values(50/75/150 ohms or disable)
- PASR(Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a $T_{CASE} 85^{\circ}C$, 3.9us at $85^{\circ}C < T_{CASE} \leq 95^{\circ}C$
- support High Temperature Self-Refresh rate enable feature
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 68ball FBGA - 256Mx4/128Mx8, 56ball BGA - st.512Mbx4
- All of Lead-free products are compliant for RoHS

Note: For detailed DDR2 SDRAM operation, please refer to Samsung's Device operation & Timing diagram..

3.0 Address Configuration

| Organization | Row Address | Column Address | Bank Address | Auto Precharge |
|--------------------------|-------------|----------------|--------------|----------------|
| 256Mx4(1Gb) based Module | A0-A13 | A0-A9, A11 | BA0-BA2 | A10 |
| 128Mx8(1Gb) based Module | A0-A13 | A0-A9 | BA0-BA2 | A10 |

4.0 Pin Configurations (Front side/Back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|------------------|-----|-----------------|-----|------------------|-----|------------------|-----|------------------|-----|------------------|-----|-----------------|-----|-----------------|
| 1 | V _{REF} | 121 | V _{SS} | 31 | DQ19 | 151 | V _{SS} | 61 | A4 | 181 | V _{DDQ} | 91 | V _{SS} | 211 | DM5/DQS14 |
| 2 | V _{SS} | 122 | DQ4 | 32 | V _{SS} | 152 | DQ28 | 62 | V _{DDQ} | 182 | A3 | 92 | DQS5 | 212 | NC/DQS14 |
| 3 | DQ0 | 123 | DQ5 | 33 | DQ24 | 153 | DQ29 | 63 | A2 | 183 | A1 | 93 | DQS5 | 213 | V _{SS} |
| 4 | DQ1 | 124 | V _{SS} | 34 | DQ25 | 154 | V _{SS} | 64 | V _{DD} | 184 | V _{DD} | 94 | V _{SS} | 214 | DQ46 |
| 5 | V _{SS} | 125 | DM0/DQS9 | 35 | V _{SS} | 155 | DM3/DQS12 | KEY | | | | 95 | DQ42 | 215 | DQ47 |
| 6 | DQS0 | 126 | NC/DQS9 | 36 | DQS3 | 156 | NC/DQS12 | 65 | V _{SS} | 185 | CK0 | 96 | DQ43 | 216 | V _{SS} |
| 7 | DQS0 | 127 | V _{SS} | 37 | DQS3 | 157 | V _{SS} | 66 | V _{SS} | 186 | CK0 | 97 | V _{SS} | 217 | DQ52 |
| 8 | V _{SS} | 128 | DQ6 | 38 | V _{SS} | 158 | DQ30 | 67 | V _{DD} | 187 | V _{DD} | 98 | DQ48 | 218 | DQ53 |
| 9 | DQ2 | 129 | DQ7 | 39 | DQ26 | 159 | DQ31 | 68 | NC/Par_In | 188 | A0 | 99 | DQ49 | 219 | V _{SS} |
| 10 | DQ3 | 130 | V _{SS} | 40 | DQ27 | 160 | V _{SS} | 69 | V _{DD} | 189 | V _{DD} | 100 | V _{SS} | 220 | RFU |
| 11 | V _{SS} | 131 | DQ12 | 41 | V _{SS} | 161 | CB4 | 70 | A10/AP | 190 | BA1 | 101 | SA2 | 221 | RFU |
| 12 | DQ8 | 132 | DQ13 | 42 | CB0 | 162 | CB5 | 71 | BA0 | 191 | V _{DDQ} | 102 | NC(TEST) | 222 | V _{SS} |
| 13 | DQ9 | 133 | V _{SS} | 43 | CB1 | 163 | V _{SS} | 72 | V _{DDQ} | 192 | RAS | 103 | V _{SS} | 223 | DM6/DQS15 |
| 14 | V _{SS} | 134 | DM1/DQS10 | 44 | V _{SS} | 164 | DM8/DQS17 | 73 | WE | 193 | S0 | 104 | DQS6 | 224 | NC/DQS15 |
| 15 | DQS1 | 135 | NC/DQS10 | 45 | DQS8 | 165 | NC/DQS17 | 74 | CAS | 194 | V _{DDQ} | 105 | DQS6 | 225 | V _{SS} |
| 16 | DQS1 | 136 | V _{SS} | 46 | DQS8 | 166 | V _{SS} | 75 | V _{DDQ} | 195 | ODT0 | 106 | V _{SS} | 226 | DQ54 |
| 17 | V _{SS} | 137 | RFU | 47 | V _{SS} | 167 | CB6 | 76 | S14 | 196 | A13 | 107 | DQ50 | 227 | DQ55 |
| 18 | RESET | 138 | RFU | 48 | CB2 | 168 | CB7 | 77 | ODT1 | 197 | V _{DD} | 108 | DQ51 | 228 | V _{SS} |
| 19 | NC | 139 | V _{SS} | 49 | CB3 | 169 | V _{SS} | 78 | V _{DDQ} | 198 | V _{SS} | 109 | V _{SS} | 229 | DQ60 |
| 20 | V _{SS} | 140 | DQ14 | 50 | V _{SS} | 170 | V _{DDQ} | 79 | V _{SS} | 199 | DQ36 | 110 | DQ56 | 230 | DQ61 |
| 21 | DQ10 | 141 | DQ15 | 51 | V _{DDQ} | 171 | CKE14 | 80 | DQ32 | 200 | DQ37 | 111 | DQ57 | 231 | V _{SS} |
| 22 | DQ11 | 142 | V _{SS} | 52 | CKE0 | 172 | V _{DD} | 81 | DQ33 | 201 | V _{SS} | 112 | V _{SS} | 232 | DM7/DQS16 |
| 23 | V _{SS} | 143 | DQ20 | 53 | V _{DD} | 173 | NC | 82 | V _{SS} | 202 | DM4/DQS13 | 113 | DQS7 | 233 | NC/DQS16 |
| 24 | DQ16 | 144 | DQ21 | 54 | BA2 | 174 | NC | 83 | DQS4 | 203 | NC/DQS13 | 114 | DQS7 | 234 | V _{SS} |
| 25 | DQ17 | 145 | V _{SS} | 55 | NC/Err_Out | 175 | V _{DDQ} | 84 | DQS4 | 204 | V _{SS} | 115 | V _{SS} | 235 | DQ62 |
| 26 | V _{SS} | 146 | DM2/DQS11 | 56 | V _{DDQ} | 176 | A12 | 85 | V _{SS} | 205 | DQ38 | 116 | DQ58 | 236 | DQ63 |
| 27 | DQS2 | 147 | NC/DQS11 | 57 | A11 | 177 | A9 | 86 | DQ34 | 206 | DQ39 | 117 | DQ59 | 237 | V _{SS} |
| 28 | DQS2 | 148 | V _{SS} | 58 | A7 | 178 | V _{DD} | 87 | DQ35 | 207 | V _{SS} | 118 | V _{SS} | 238 | VDDSPD |
| 29 | V _{SS} | 149 | DQ22 | 59 | V _{DD} | 179 | A8 | 88 | V _{SS} | 208 | DQ44 | 119 | SDA | 239 | SA0 |
| 30 | DQ18 | 150 | DQ23 | 60 | A5 | 180 | A6 | 89 | DQ40 | 209 | DQ45 | 120 | SCL | 240 | SA1 |
| | | | | | | | | 90 | DQ41 | 210 | V _{SS} | | | | |

NC = No Connect, RFU = Reserved for Future Use

1. RESET (Pin 18) is connected to both OE of PLL and Reset of register.
2. The Test pin (Pin 102) is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)
3. NC/Err_Out (Pin 55) and NC/Par_In (Pin 68) are for optional function to check address and command parity.
4. CKE1,S1 Pin is used for double side Registered DIMM.

5.0 Pin Description

| Pin Name | Description | Pin Name | Description |
|----------------|---|--------------------|--|
| CK0 | Clock Inputs, positive line | ODT0~ODT1 | On die termination |
| CK0 | Clock inputs, negative line | DQ0~DQ63 | Data Input/Output |
| CKE0, CKE1 | Clock Enables | CB0~CB7 | Data check bits Input/Output |
| RAS | Row Address Strobe | DQS0~DQS8 | Data strobes |
| CAS | Column Address Strobe | DQS0~DQS8 | Data strobes, negative line |
| WE | Write Enable | DM(0~8), DQS(9~17) | Data Masks / Data strobes (Read) |
| S0, S1 | Chip Selects | DQS9~DQS17 | Data strobes (Read), negative line |
| A0~A9, A11~A13 | Address Inputs | RFU | Reserved for Future Use |
| A10/AP | Address Input/Autoprecharge | NC | No Connect |
| BA0~BA2 | DDR2 SDRAM Bank Address | TEST | Memory bus test tool (Not Connect and Not Useable on DIMMs) |
| SCL | Serial Presence Detect (SPD) Clock Input | V _{DD} | Core Power |
| SDA | SPD Data Input/Output | V _{DDQ} | I/O Power |
| SA0~SA2 | SPD address | V _{SS} | Ground |
| Par_In | Parity bit for the Address and Control bus | V _{REF} | Input/Output Reference |
| Err_Out | Parity error found in the Address and Control bus | V _{DDSPD} | SPD Power |
| RESET | Register and PLL control pin | | |

* The VDD and VDDQ pins are tied to the single power-plane on PCB.

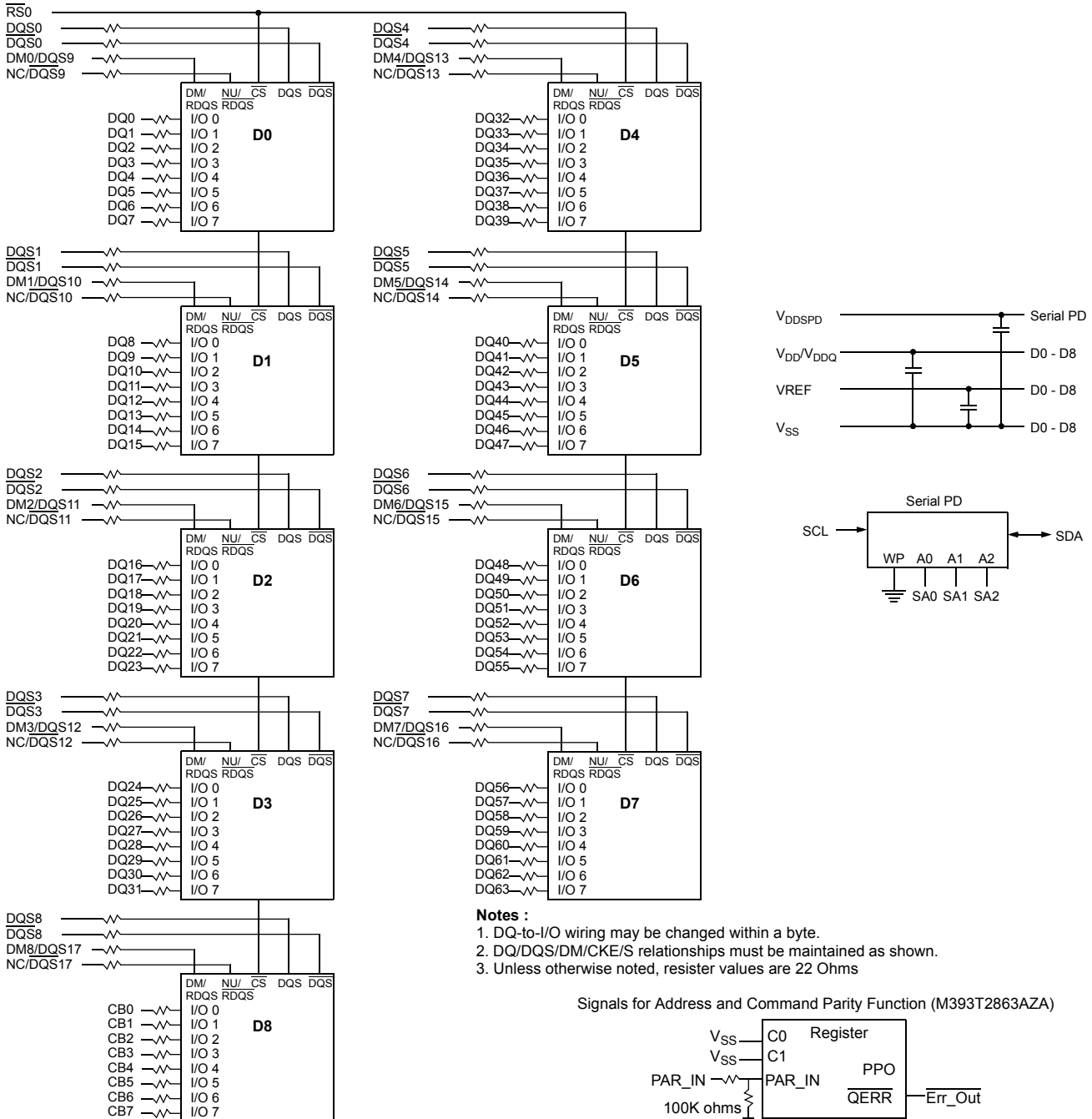
6.0 Input/Output Function Description

| Symbol | Type | Description |
|--|--------|--|
| CK0 | Input | Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL. |
| $\overline{\text{CK0}}$ | Input | Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL. |
| CKE0~CKE1 | Input | Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. |
| $\overline{\text{S0}}\text{~}\overline{\text{S1}}$ | Input | Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. |
| ODT0~ODT1 | Input | I/O bus impedance control signals. |
| $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ | Input | When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM. |
| V _{REF} | Supply | Reference voltage for SSTL_18 inputs |
| V _{DDQ} | Supply | Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity |
| BA0~BA2 | Input | Selects which SDRAM bank of eight is activated. |
| A0~A9,A10/AP A11~A13 | Input | During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge. |
| DQ0~63, CB0~CB7 | In/Out | Data and Check Bit Input/Output pins |
| DM0~DM8 | Input | Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM. |
| V _{DD} , V _{SS} | Supply | Power and ground for the DDR SDRAM input buffers and core logic |
| DQS0~DQS17 | In/Out | Positive line of the differential data strobe for input and output data. |
| $\overline{\text{DQS0}}\text{~}\overline{\text{DQS17}}$ | In/Out | Negative line of the differential data strobe for input and output data. |
| SA0~SA2 | Input | These signals are tied at the system planar to either V _{SS} or V _{DDSPD} to configure the serial SPD EEPROM address range. |
| SDA | In/Out | This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V _{DDSPD} to act as a pullup. |
| SCL | Input | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V _{DDSPD} to act as a pullup. |
| V _{DDSPD} | Supply | Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt operation). |
| $\overline{\text{RESET}}$ | Input | The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (The PLL will remain synchronized with the input clock) |
| Par_In | Input | Parity bit for the Address and Control bus. ("1 " : Odd, "0 " : Even) |
| $\overline{\text{Err_Out}}$ | Output | Parity error found in the Address and Control bus |
| TEST | In/Out | Used by memory bus analysis tools (unused on memory DIMMs) |

7.0 Functional Block Diagram

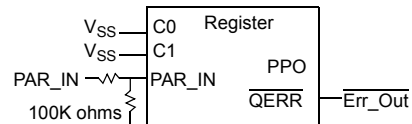
7.1 1GB, 128Mx72 Module (M393T2863AZ3/M393T2863AZA)

(populated as 1 rank of x8 DDR2 SDRAMs)

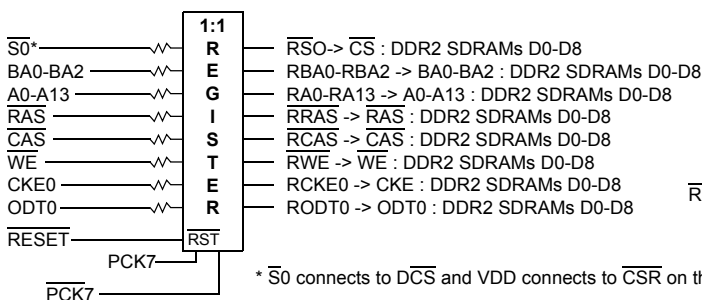


- Notes :**
1. DQ-to-I/O wiring may be changed within a byte.
 2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
 3. Unless otherwise noted, resistor values are 22 Ohms

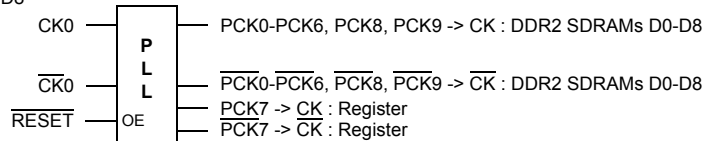
Signals for Address and Command Parity Function (M393T2863AZA)



The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"

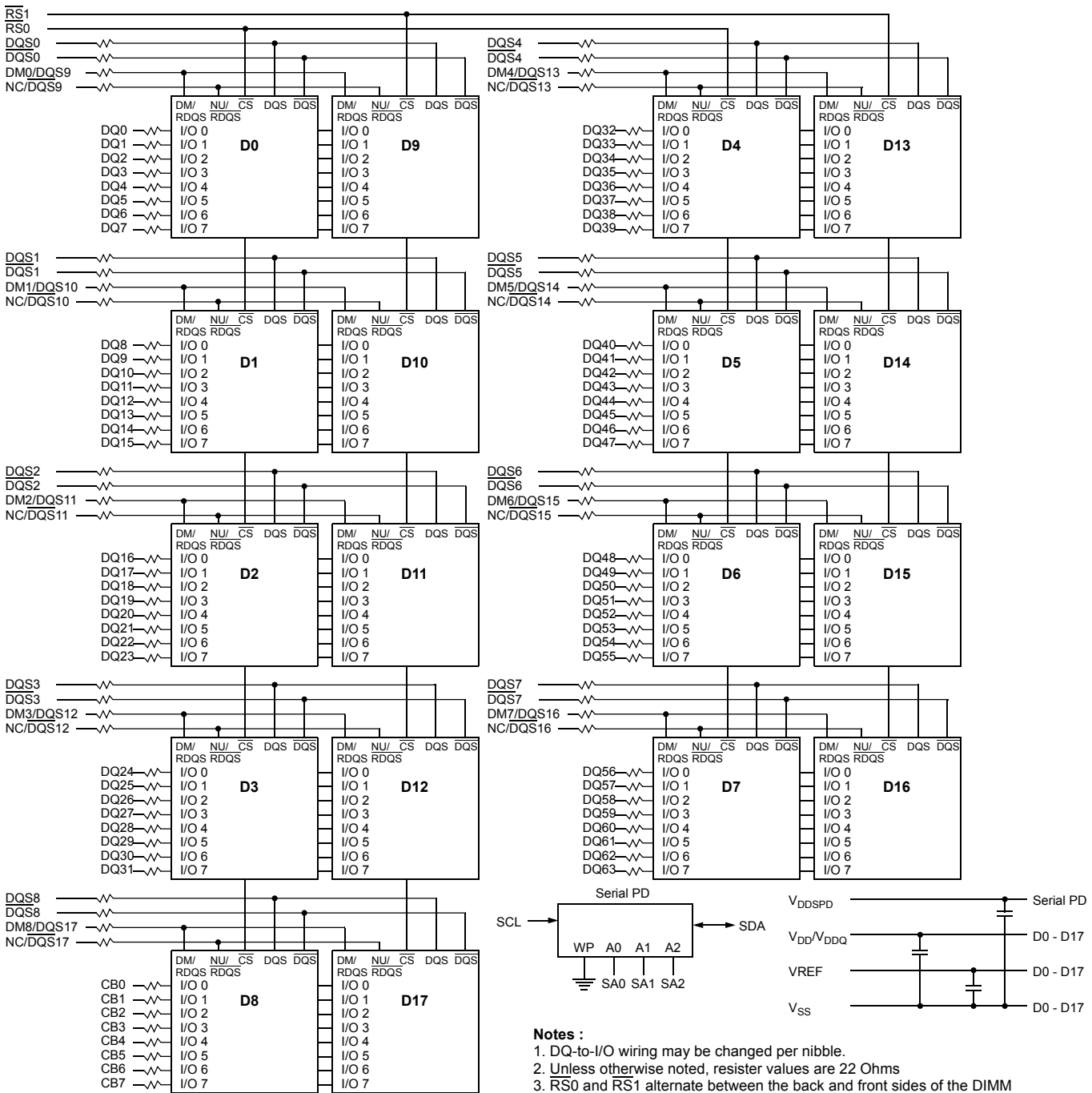


* $\bar{S}0$ connects to \overline{DCS} and VDD connects to \overline{CSR} on the register. $\bar{S}1$, CKE1 and ODT are NC.



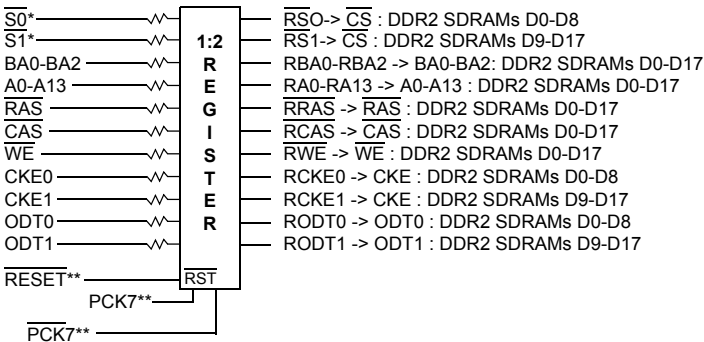
7.2 2GB, 256Mx72 Module (M393T5663AZ3/M393T5663AZA)

(populated as 2 rank of x8 DDR2 SDRAMs)



Notes :

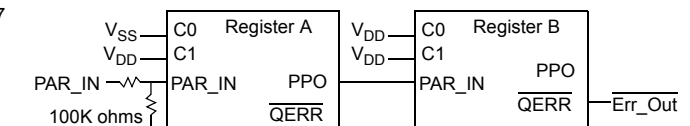
1. DQ-to-I/O wiring may be changed per nibble.
2. Unless otherwise noted, resistor values are 22 Ohms
3. RS0 and RS1 alternate between the back and front sides of the DIMM



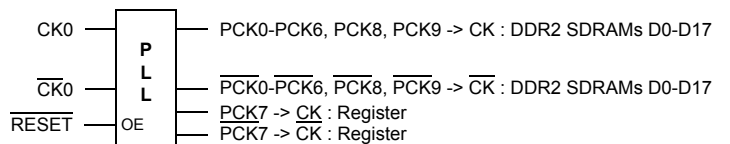
* S0 connects to DCS and S1 connects to CSR on a Register, S1 connects to DCS and S0 connects to CSR on another Register.

** RESET, PCK7 and PCK7 connects to both Registers. Other signals connect to one of two Registers.

Signals for Address and Command Parity Function (M393T5663AZA)

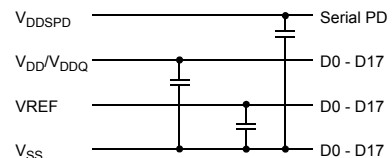
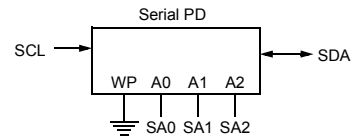
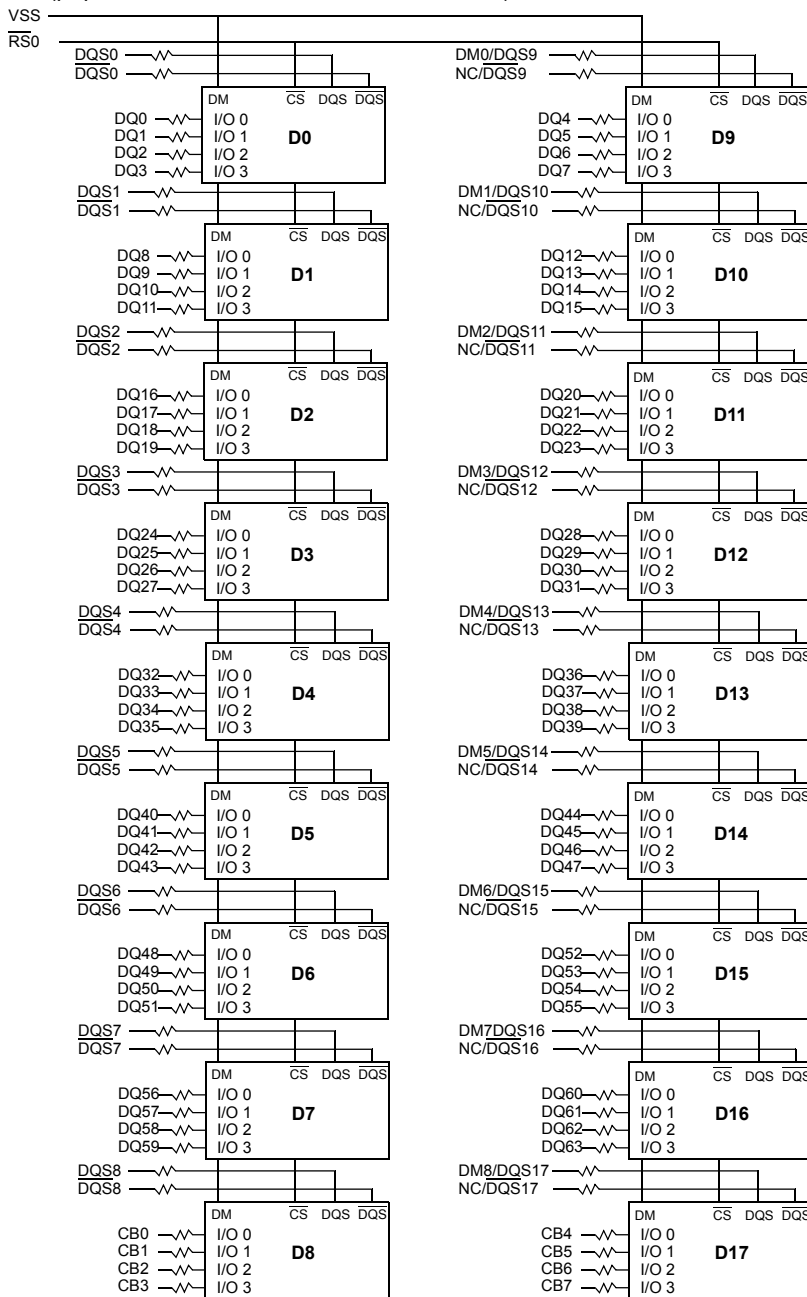


The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"

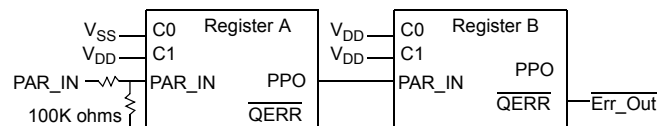


7.3 2GB, 256Mx72 Module (M393T5660AZ3/M393T5660AZA)

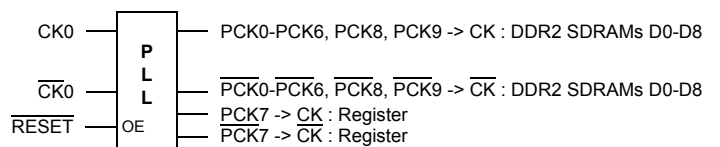
(populated as 1 rank of x4 DDR2 SDRAMs)



Signals for Address and Command Parity Function (M393T5660AZA)

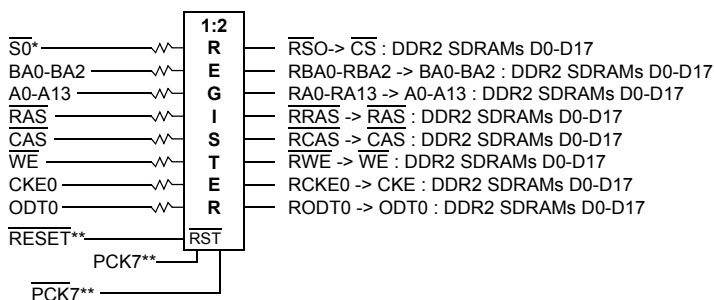


The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"



Notes :

1. DQ-to-I/O wiring may be changed per nibble.
2. Unless otherwise noted, resistor values are 22 Ohms



* S0 connects to DCS of Register1 and CSR of Register2. CSR of register 1 and DCS of register 2 connects to VDD.

** RESET, PCK7 and PCK7 connects to both Registers. Other signals connect to one of two Registers. S1, CKE1 and ODT1 are NC.

8.0 Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Notes |
|------------------------------------|---|-----------------|-------|-------|
| V _{DD} | Voltage on V _{DD} pin relative to V _{SS} | - 1.0 V ~ 2.3 V | V | 1 |
| V _{DDQ} | Voltage on V _{DDQ} pin relative to V _{SS} | - 0.5 V ~ 2.3 V | V | 1 |
| V _{DDL} | Voltage on V _{DDL} pin relative to V _{SS} | - 0.5 V ~ 2.3 V | V | 1 |
| V _{IN} , V _{OUT} | Voltage on any pin relative to V _{SS} | - 0.5 V ~ 2.3 V | V | 1 |
| T _{STG} | Storage Temperature | -55 to +100 | °C | 1, 2 |

Note :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

9.0 AC & DC Operating Conditions

Recommended DC Operating Conditions (SSTL - 1.8)

| Symbol | Parameter | Rating | | | Units | Notes |
|------------------|---------------------------|------------------------|-----------------------|------------------------|-------|-------|
| | | Min. | Typ. | Max. | | |
| V _{DD} | Supply Voltage | 1.7 | 1.8 | 1.9 | V | |
| V _{DDL} | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 4 |
| V _{DDQ} | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 4 |
| V _{REF} | Input Reference Voltage | 0.49*V _{DDQ} | 0.50*V _{DDQ} | 0.51*V _{DDQ} | mV | 1,2 |
| V _{TT} | Termination Voltage | V _{REF} -0.04 | V _{REF} | V _{REF} +0.04 | V | 3 |

Note : There is no specific device V_{DD} supply voltage requirement for SSTL-1.8 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.

- The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
- Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF}(DC).
- V_{TT} of transmitting device must track V_{REF} of receiving device.
- AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

9.1 Operating Temperature Condition

| Symbol | Parameter | Rating | Units | Notes |
|--------|-----------------------|---------|-------|---------|
| TOPER | Operating Temperature | 0 to 95 | °C | 1, 2, 3 |

Note :

- Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
- At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

9.2 Input DC Logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|----------------------|---------------------|--------------------------|--------------------------|-------|-------|
| V _{IH} (DC) | DC input logic high | V _{REF} + 0.125 | V _{DDQ} + 0.3 | V | |
| V _{IL} (DC) | DC input logic low | - 0.3 | V _{REF} - 0.125 | V | |

9.3 Input AC Logic Level

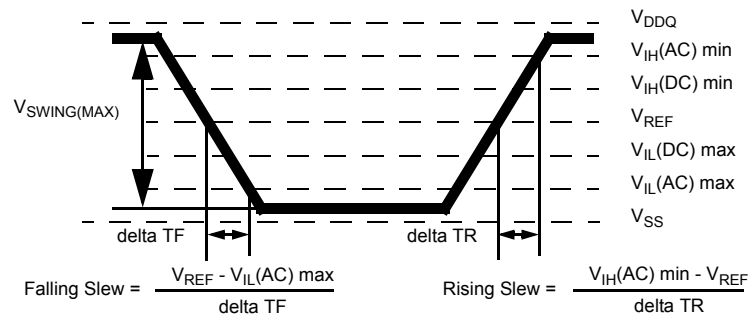
| Symbol | Parameter | DDR2-400, DDR2-533 | | DDR2-667 | | Units |
|----------------------|---------------------|--------------------------|--------------------------|--------------------------|--------------------------|-------|
| | | Min. | Max. | Min. | Max. | |
| V _{IH} (AC) | AC input logic high | V _{REF} + 0.250 | - | V _{REF} + 0.200 | - | V |
| V _{IL} (AC) | AC input logic low | - | V _{REF} - 0.250 | - | V _{REF} - 0.200 | V |

9.4 AC Input Test Conditions

| Symbol | Condition | Value | Units | Notes |
|-------------------------|---|------------------------|-------|-------|
| V _{REF} | Input reference voltage | 0.5 * V _{DDQ} | V | 1 |
| V _{SWING(MAX)} | Input signal maximum peak to peak swing | 1.0 | V | 1 |
| SLEW | Input signal minimum slew rate | 1.0 | V/ns | 2, 3 |

Notes:

- Input waveform timing is referenced to the input signal crossing through the V_{IH/IL}(AC) level applied to the device under test.
- The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
- AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.



< AC Input Test Signal Waveform >

10.0 IDD Specification Parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

| Symbol | Proposed Conditions | Units | Note |
|--------|---|-----------------------------|------|
| IDD0 | Operating one bank active-precharge current; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RASmin}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD1 | Operating one bank active-read-precharge current; $I_{OUT} = 0mA$; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RASmin}(IDD)$, $t_{RCD} = t_{RCD}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | mA | |
| IDD2P | Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | mA | |
| IDD2Q | Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | mA | |
| IDD2N | Precharge standby current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD3P | Active power-down current; All banks open; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | Fast PDN Exit MRS(12) = 0mA | mA |
| | | Slow PDN Exit MRS(12) = 1mA | mA |
| IDD3N | Active standby current; All banks open; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD4W | Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD4R | Operating burst read current; All banks open, Continuous burst reads, $I_{OUT} = 0mA$; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | mA | |
| IDD5B | Burst auto refresh current; $t_{CK} = t_{CK}(IDD)$; Refresh command at every $t_{RFC}(IDD)$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD6 | Self refresh current; CK and CK\ at 0V; CKE $\leq 0.2V$; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | Normal | mA |
| | | Low Power | mA |
| IDD7 | Operating bank interleave read current; All bank interleaving reads, $I_{OUT} = 0mA$; BL = 4, CL = CL(IDD), AL = $t_{RCD}(IDD) - 1 * t_{CK}(IDD)$; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RRD} = t_{RRD}(IDD)$, $t_{FAW} = t_{FAW}(IDD)$, $t_{RCD} = 1 * t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions | mA | |

11.0 Operating Current Table(1-1)

11.1 M393T2863AZ3/M393T2863AZA : 1GB(128Mx8 *9) Module

(TA=0°C, VDD= 1.9V)

| Symbol | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---------|--------------------|--------------------|--------------------|------|-------|
| IDD0 | 1,310 | 1,175 | 1,085 | mA | |
| IDD1 | 1,450 | 1,315 | 1,225 | mA | |
| IDD2P | 575 | 535 | 495 | mA | |
| IDD2Q | 865 | 795 | 680 | mA | |
| IDD2N | 825 | 765 | 660 | mA | |
| IDD3P-F | 830 | 705 | 625 | mA | |
| IDD3P-S | 632 | 552 | 472 | mA | |
| IDD3N | 1,010 | 940 | 825 | mA | |
| IDD4W | 1,845 | 1,550 | 1,345 | mA | |
| IDD4R | 1,905 | 1,600 | 1,385 | mA | |
| IDD5B | 2,530 | 2,365 | 2,200 | mA | |
| IDD6* | Normal | 135 | 135 | mA | |
| IDD7 | 3,280 | 2,990 | 2,700 | mA | |

* IDD6 = DRAM current + standby current of PLL and Register

** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.2 M393T5663AZ3/M393T5663AZA : 2GB(128Mx8 *18) Module

(TA=0°C, VDD= 1.9V)

| Symbol | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---------|--------------------|--------------------|--------------------|------|-------|
| IDD0 | 1,805 | 1,660 | 1,515 | mA | |
| IDD1 | 1,965 | 1,810 | 1,655 | mA | |
| IDD2P | 850 | 790 | 730 | mA | |
| IDD2Q | 1,430 | 1,340 | 1,160 | mA | |
| IDD2N | 1,310 | 1,240 | 1,080 | mA | |
| IDD3P-F | 1,350 | 1,160 | 1,060 | mA | |
| IDD3P-S | 954 | 854 | 754 | mA | |
| IDD3N | 1,435 | 1,365 | 1,205 | mA | |
| IDD4W | 2,360 | 2,045 | 1,775 | mA | |
| IDD4R | 2,480 | 2,145 | 1,855 | mA | |
| IDD5B | 3,065 | 2,870 | 2,630 | mA | |
| IDD6* | Normal | 270 | 270 | mA | |
| IDD7 | 3,975 | 3,635 | 3,250 | mA | |

* IDD6 = DRAM current + standby current of PLL and Register

** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.3 M393T5660AZ3/M393T5660AZA : 2GB(256Mx4 *18) Module

(TA=0°C, VDD= 1.9V)

| Symbol | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---------|--------------------|--------------------|--------------------|-------|-------|
| IDD0 | 2,210 | 2,020 | 1,920 | mA | |
| IDD1 | 2,460 | 2,260 | 2,150 | mA | |
| IDD2P | 850 | 790 | 730 | mA | |
| IDD2Q | 1,430 | 1,340 | 1,160 | mA | |
| IDD2N | 1,310 | 1,240 | 1,080 | mA | |
| IDD3P-F | 1,350 | 1,160 | 1,060 | mA | |
| IDD3P-S | 954 | 854 | 754 | mA | |
| IDD3N | 1,570 | 1,500 | 1,340 | mA | |
| IDD4W | 2,990 | 2,630 | 2,180 | mA | |
| IDD4R | 3,110 | 2,730 | 2,260 | mA | |
| IDD5B | 4,640 | 4,400 | 4,160 | mA | |
| IDD6* | Normal | 270 | 270 | mA | |
| IDD7 | | 6,270 | 5,750 | 5,230 | mA |

* IDD6 = DRAM current + standby current of PLL and Register

** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.4 M393T5168AZ0/M393T5166AZA : 4GB(st.512Mx4 *18) Module

(TA=0°C, VDD= 1.9V)

| Symbol | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---------|--------------------|--------------------|--------------------|-------|-------|
| IDD0 | 3,300 | 3,060 | 2,820 | mA | |
| IDD1 | 3,610 | 3,360 | 3,110 | mA | |
| IDD2P | 1,400 | 1,310 | 1,220 | mA | |
| IDD2Q | 2,540 | 2,400 | 2,080 | mA | |
| IDD2N | 2,320 | 2,220 | 1,940 | mA | |
| IDD3P-F | 2,380 | 2,050 | 1,900 | mA | |
| IDD3P-S | 1,588 | 1,438 | 1,288 | mA | |
| IDD3N | 2,580 | 2,480 | 2,200 | mA | |
| IDD4W | 4,090 | 3,680 | 3,090 | mA | |
| IDD4R | 4,180 | 3,760 | 3,160 | mA | |
| IDD5B | 5,770 | 5,460 | 5,060 | mA | |
| IDD6* | Normal | 540 | 540 | mA | |
| IDD7 | | 7,660 | 7,040 | 6,330 | mA |

* IDD6 = DRAM current + standby current of PLL and Register

** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

12.0 Input/Output Capacitance

(V_{DD}=1.8V, V_{DDQ}=1.8V, T_A=25°C)

| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Units |
|--|--------|------------------------------|------------------------------|------------------------------|------------------------------|-----|-----|-----|-----|-------|
| Part-Number | | M393T2863AZ3 M393T2863AZA | M393T5663AZ3 M393T5663AZA | M393T5660AZ3 M393T5660AZA | M393T5168AZ0 M393T5166AZA | | | | | |
| Input capacitance, CK and \overline{CK} | CCK | - | 11 | - | 11 | - | 11 | - | 11 | pF |
| Input capacitance, CKE and \overline{CS} | CI1 | - | 12 | - | 12 | - | 12 | - | 12 | |
| Input capacitance, Addr, \overline{RAS} , \overline{CAS} , \overline{WE} | CI2 | - | 12 | - | 12 | - | 12 | - | 12 | |
| Input/output capacitance, DQ, DM, DQS, \overline{DQS} | CIO | - | 10 | - | 10 | - | 10 | - | 10 | |

* DM is internally loaded to match DQ and DQS identically.

13.0 Electrical Characteristics & AC Timing for DDR2-667/533/400

(0 °C ≤ T_{OPER} ≤ 95 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

13.1 Refresh Parameters by Device Density

| Parameter | Symbol | 256Mb | 512Mb | 1Gb | 2Gb | 4Gb | Units | |
|--|--------|----------------------------------|-------|-------|-----|-------|-------|----|
| Refresh to active/Refresh command time | tRFC | 75 | 105 | 127.5 | 195 | 327.5 | ns | |
| Average periodic refresh interval | tREFI | 0 °C ≤ T _{CASE} ≤ 85°C | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | μs |
| | | 85 °C < T _{CASE} ≤ 95°C | 3.9 | 3.9 | 3.9 | 3.9 | 3.9 | μs |

13.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

| Speed | DDR2-667(E6) | | DDR2-533(D5) | | DDR2-400(CC) | | Units |
|----------------------|--------------|-------|--------------|-------|--------------|-------|-------|
| Bin(CL - tRCD - tRP) | 5 - 5 - 5 | | 4 - 4 - 4 | | 3 - 3 - 3 | | |
| Parameter | min | max | min | max | min | max | |
| tCK, CL=3 | 5 | 8 | 5 | 8 | 5 | 8 | ns |
| tCK, CL=4 | 3.75 | 8 | 3.75 | 8 | 5 | 8 | ns |
| tCK, CL=5 | 3 | 8 | - | - | - | - | ns |
| tRCD | 15 | - | 15 | - | 15 | - | ns |
| tRP | 15 | - | 15 | - | 15 | - | ns |
| tRC | 54 | - | 55 | - | 55 | - | ns |
| tRAS | 39 | 70000 | 40 | 70000 | 40 | 70000 | ns |

13.3 Timing Parameters by Speed Grade

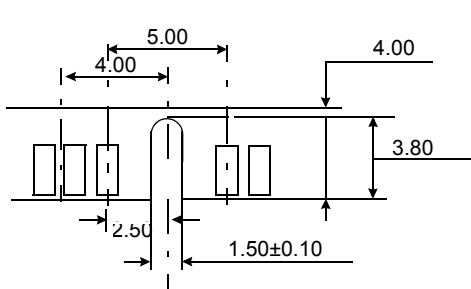
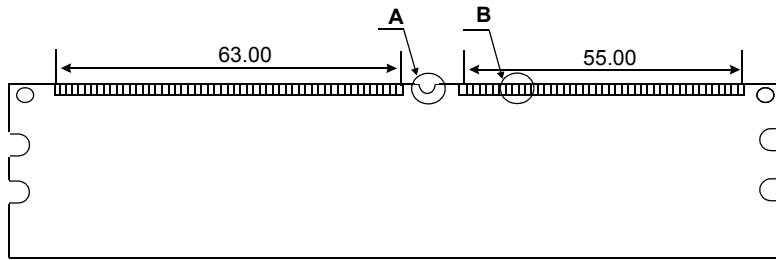
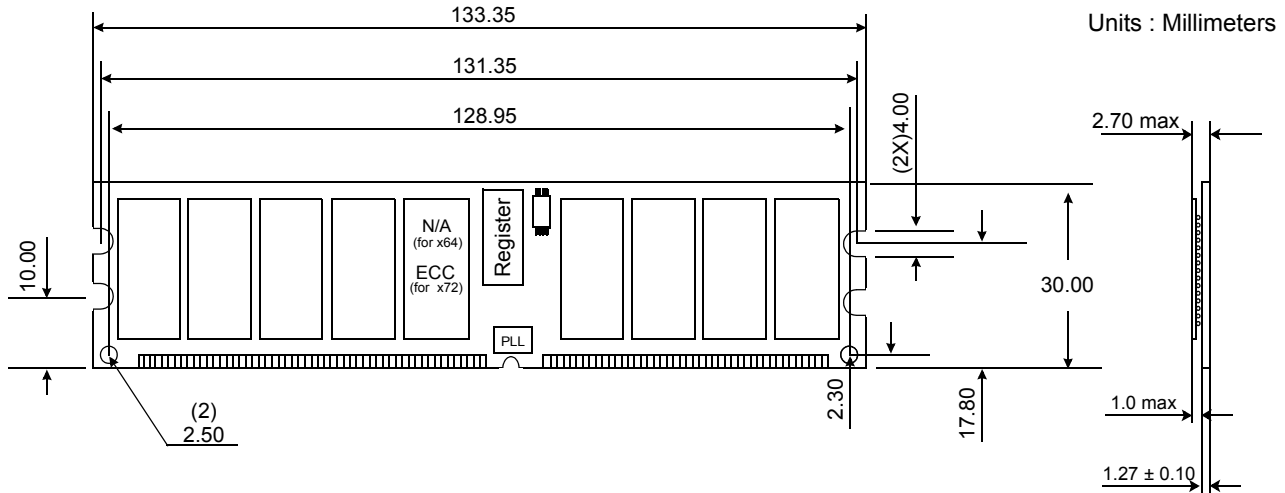
(Refer to notes for informations related to this table at the bottom)

| Parameter | Symbol | DDR2-667 | | DDR2-533 | | DDR2-400 | | Units | Notes |
|--|----------|---------------|---------|---------------|---------|---------------|---------|-------|-------|
| | | min | max | min | max | min | max | | |
| DQ output access time from CK/CK | tAC | -450 | +450 | -500 | +500 | -600 | +600 | ps | |
| DQS output access time from CK/CK | tDQSCK | -400 | +400 | -450 | +450 | -500 | +500 | ps | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK half period | tHP | min(tCL, tCH) | x | min(tCL, tCH) | x | min(tCL, tCH) | x | ps | |
| Clock cycle time, CL=x | tCK | 3000 | 8000 | 3750 | 8000 | 5000 | 8000 | ps | |
| DQ and DM input hold time | tDH | 175 | x | 225 | x | 275 | x | ps | |
| DQ and DM input setup time | tDS | 100 | x | 100 | x | 150 | x | ps | |
| Control & Address input pulse width for each input | tIPW | 0.6 | x | 0.6 | x | 0.6 | x | tCK | |
| DQ and DM input pulse width for each input | tDIPW | 0.35 | x | 0.35 | x | 0.35 | x | tCK | |
| Data-out high-impedance time from CK/CK | tHZ | x | tAC max | x | tAC max | x | tAC max | ps | |
| DQS low-impedance time from CK/CK | tLZ(DQS) | tAC min | tAC max | tAC min | tAC max | tAC min | tAC max | ps | |
| DQ low-impedance time from CK/CK | tLZ(DQ) | 2*tAC min | tAC max | 2* tACmin | tAC max | 2* tACmin | tAC max | ps | |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | x | 240 | x | 300 | x | 350 | ps | |
| DQ hold skew factor | tQHS | x | 340 | x | 400 | x | 450 | ps | |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | x | tHP - tQHS | x | tHP - tQHS | x | ps | |
| Write command to first DQS latching transition | tDQSS | -0.25 | 0.25 | -0.25 | 0.25 | -0.25 | 0.25 | tCK | |

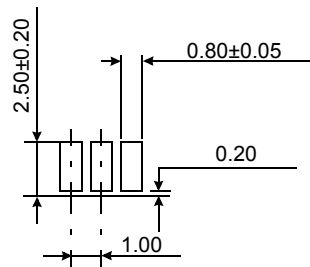
| Parameter | Symbol | DDR2-667 | | DDR2-533 | | DDR2-400 | | Units | Notes |
|---|--------|-------------|-------------------|-------------|-------------------|-------------|-------------------|-------|-------|
| | | min | max | min | max | min | max | | |
| DQS input high pulse width | tDQSH | 0.35 | x | 0.35 | x | 0.35 | x | tCK | |
| DQS input low pulse width | tDQSL | 0.35 | x | 0.35 | x | 0.35 | x | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | x | 0.2 | x | 0.2 | x | tCK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | x | 0.2 | x | 0.2 | x | tCK | |
| Mode register set command cycle time | tMRD | 2 | x | 2 | x | 2 | x | tCK | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Write preamble | tWPRE | 0.35 | x | 0.35 | x | 0.35 | x | tCK | |
| Address and control input hold time | tIH | 275 | x | 375 | x | 475 | x | ps | |
| Address and control input setup time | tIS | 200 | x | 250 | x | 350 | x | ps | |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Active to active command period for 1KB page size products | tRRD | 7.5 | x | 7.5 | x | 7.5 | x | ns | |
| Active to active command period for 2KB page size products | tRRD | 10 | x | 10 | x | 10 | x | ns | |
| Four Activate Window for 1KB page size products | tFAW | 37.5 | | 37.5 | | 37.5 | | ns | |
| Four Activate Window for 2KB page size products | tFAW | 50 | | 50 | | 50 | | ns | |
| CAS to $\overline{\text{CAS}}$ command delay | tCCD | 2 | | 2 | | 2 | | tCK | |
| Write recovery time | tWR | 15 | x | 15 | x | 15 | x | ns | |
| Auto precharge write recovery + precharge time | tDAL | WR+tRP | x | tWR+tRP | x | tWR+tRP | x | tCK | |
| Internal write to read command delay | tWTR | 7.5 | x | 7.5 | x | 10 | x | ns | |
| Internal read to precharge command delay | tRTP | 7.5 | | 7.5 | | 7.5 | | ns | |
| Exit self refresh to a non-read command | tXSNR | tRFC + 10 | | tRFC + 10 | | tRFC + 10 | | ns | |
| Exit self refresh to a read command | tXSRD | 200 | | 200 | | 200 | | tCK | |
| Exit precharge power down to any non-read command | tXP | 2 | x | 2 | x | 2 | x | tCK | |
| Exit active power down to read command | tXARD | 2 | x | 2 | x | 2 | x | tCK | |
| Exit active power down to read command (Slow exit, Lower power) | tXARDS | 7 - AL | | 6 - AL | | 6 - AL | | tCK | |
| CKE minimum pulse width (high and low pulse width) | tCKE | 3 | | 3 | | 3 | | tCK | |
| ODT turn-on delay | tAOND | 2 | 2 | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | tAON | tAC(min) | tAC(max)+0.7 | tAC(min) | tAC(max)+1 | tAC(min) | tAC(max)+1 | ns | |
| ODT turn-on (Power-Down mode) | tAONPD | tAC(min)+2 | 2tCK+tAC(max)+1 | tAC(min)+2 | 2tCK+tAC(max)+1 | tAC(min)+2 | 2tCK+tAC(max)+1 | ns | |
| ODT turn-off delay | tAOFD | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | tAOF | tAC(min) | tAC(max)+0.6 | tAC(min) | tAC(max)+0.6 | tAC(min) | tAC(max)+0.6 | ns | |
| ODT turn-off (Power-Down mode) | tAOFPD | tAC(min)+2 | 2.5tCK+tAC(max)+1 | tAC(min)+2 | 2.5tCK+tAC(max)+1 | tAC(min)+2 | 2.5tCK+tAC(max)+1 | ns | |
| ODT to power down entry latency | tANPD | 3 | | 3 | | 3 | | tCK | |
| ODT power down exit latency | tAXPD | 8 | | 8 | | 8 | | tCK | |
| OCD drive mode output delay | tOIT | 0 | 12 | 0 | 12 | 0 | 12 | ns | |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | tIS+tCK+tIH | | tIS+tCK+tIH | | tIS+tCK+tIH | | ns | |

14.0 Physical Dimensions

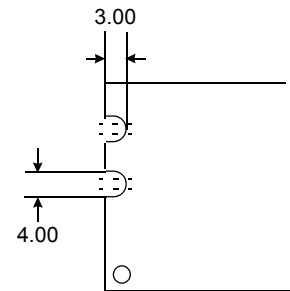
14.1 128Mbx8 based 128Mx72 Module(1 Rank) (M393T2863AZ3/M393T2863AZA)



Detail A



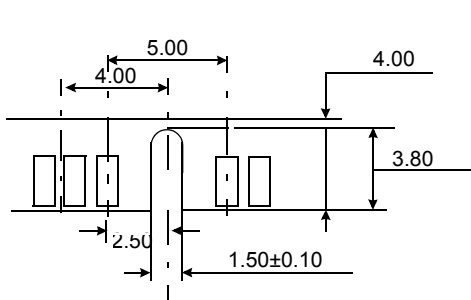
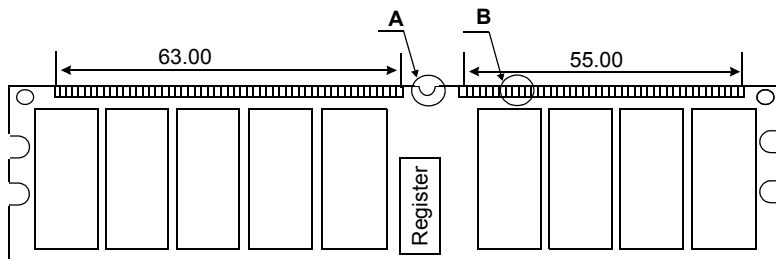
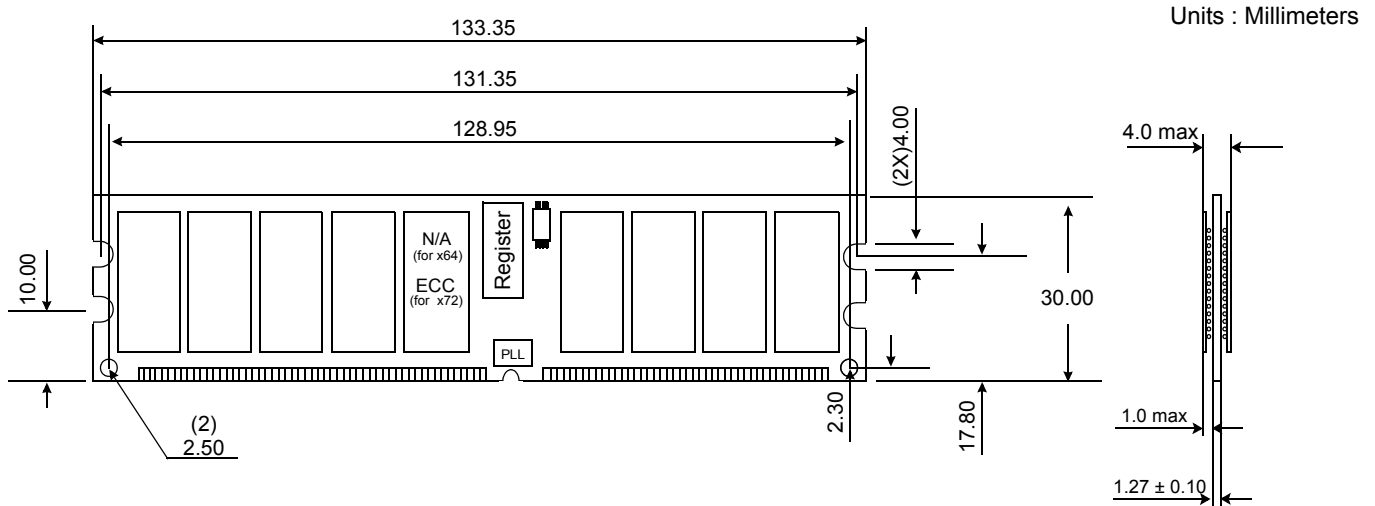
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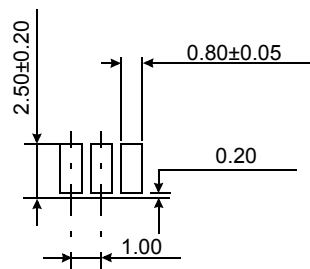
The used device is 128M x8 DDR2 SDRAM, FBGA.
 DDR2 SDRAM Part NO : K4T1G084QA

14.2 128Mbx8/256Mbx4 based 256Mx72 Module(2/1 Ranks)

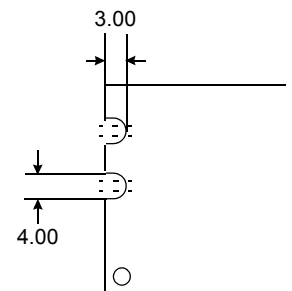
(M393T5663AZ3 / M393T5663AZA / M393T5660AZ3 / M393T5660AZA)



Detail A

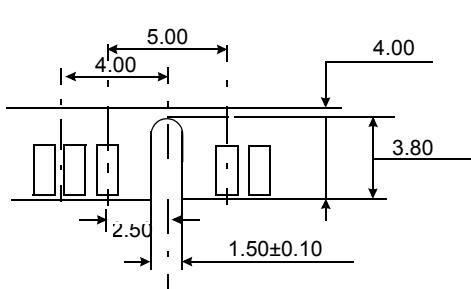
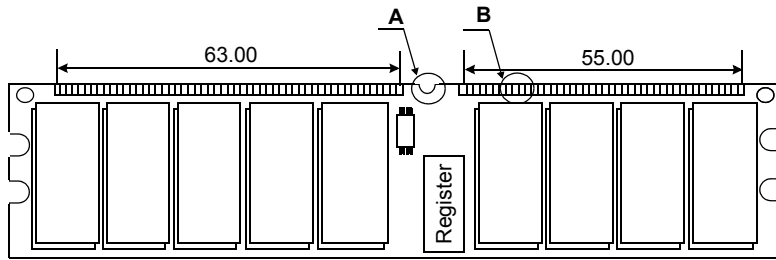
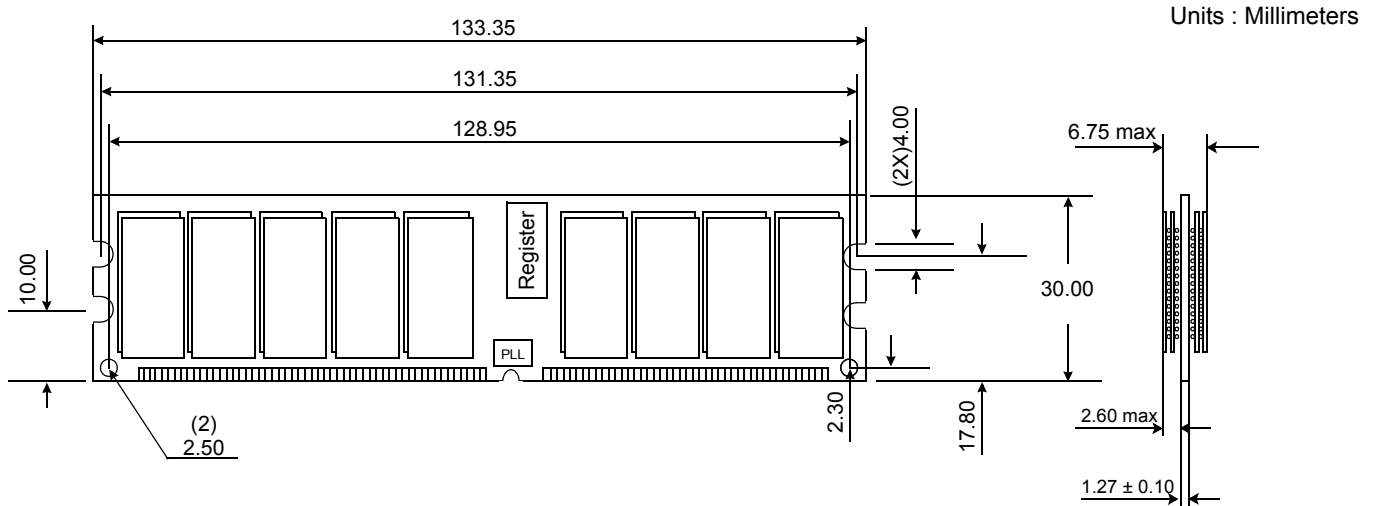


Detail B

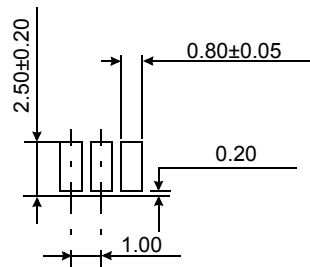


The used device is 128M x8 / 256M x4 DDR2 SDRAM, FBGA.
 DDR2 SDRAM Part NO : K4T1G084QA / K4T1G044QA

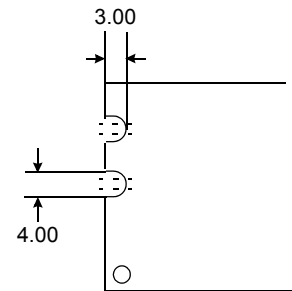
14.3 st.512Mbx4 based 512Mx72 Module(2 Ranks) (M393T5168AZ0/M393T5166AZA)



Detail A

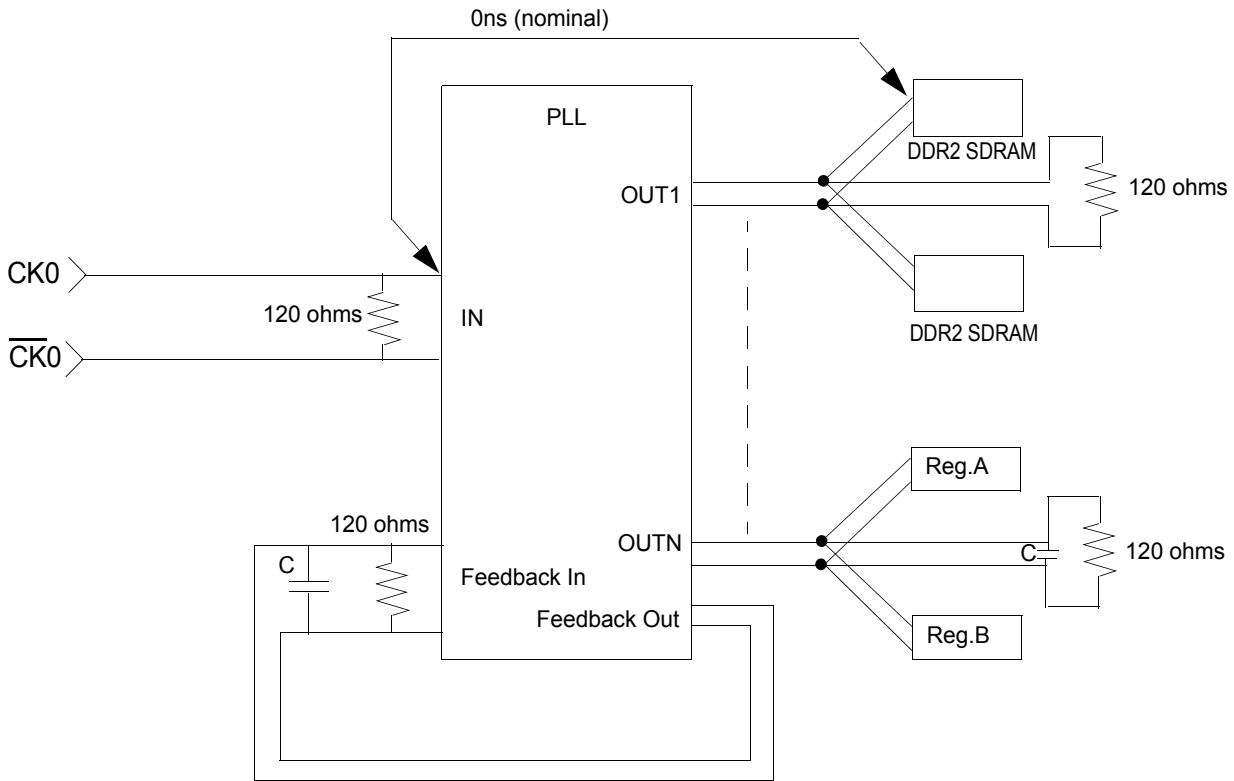


Detail B



The used device is st.512M x4 DDR2 SDRAM.
 DDR2 SDRAM Part NO : K4T2G064QA / K4T2G264QA

15.0 240 Pin DDR2 Registered DIMM Clock Topology



Note :

1. The clock delay from the input of the PLL clock to the input of any DDR2 SDRAM or register will be set to 0ns (nominal).
2. Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.